Notice of Allowability	Application No.	Applicant(s)	
	10/020,511	WILLIAMS ET AL.	
	Examiner	Art Unit	
	Matthew A. Henry	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/18/2001*.

2. ☒ The allowed claim(s) is/are *1-27*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because Figures 1-5 are either hand drawn or have hand-written components and thus lack clarity. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Allowable Subject Matter

2. Claims 1-27 are allowed.

3. The following is an examiner's statement of reasons for allowance:

Concerning Claim 1, Yoshida discloses:

A data processing apparatus (Column 4, Lines 62-63), comprising:

a processor (Column 5, Lines 12-14) for executing data processing instructions including power management instructions (Table 11, Columns 24, Lines 52-53), at least one of said power management instructions being a command power management instruction (Table 11);

a power management controller (Figure 1, Item PR; Column 4, Lines 62-65) for receiving command data from the processor when a command power management instruction is executed by the processor (Column 5, Lines 15-16), and to control power management logic to perform an associated set of power management functions dependent on said command data (Column 5, Lines 8-11);

first power management logic controllable by the power management controller (Column 5, Lines 32-36);

the power management controller having an interface to enable communication with additional power management logic (Figure Column 5, Lines 32-36);

Yoshida does not disclose an emulation mode for the power management controller. As a result, he does not disclose the processor being able to affect both the power management functions and the emulation mode of the power management controller according to a power management instruction. Nor does Yoshida disclose the power management functions executed being dependent upon the emulation mode of the power management controller.

Gaglani teaches:

said power management controller (Columns 2 and 5-6, Lines 27-30 and 65-67 to 1, respectively; although Gaglani does not specifically teach of a power management controller, he extends his teachings to other circuits, of which a power management controller may be included without changing the principles behind his teachings) being arranged when said emulation mode is not set to initiate said associated set of power management functions dependent on said command data (Figure 3A; Column 5, Lines 12-29), and being arranged when said emulation mode is set to only initiate a subset of said associated set of power management functions not requiring communication over said interface (Column 6, Lines 10-15).

Gaglani provides as partial motivation that "one objective of testing is providing individual access to the carious functionalities and hardware elements of the device, so that the performance characteristics thereof can be evaluated" (Column 1, Lines 35-38). Although Gaglani does not cite a power management controller, it is clear that the principles he expresses in his motivate that his teachings may be applied to a power management controller in a data processing apparatus. Therefore, it would have been obvious to a person of ordinary skill in the

art to combine the teachings of Gaglani with the device disclosed by Yoshida for the purposes of providing a simple way for testing the correctness of the power management controller.

Gaglani, however, does not teach of affecting both the operation of the circuit as well as the emulation mode of the circuit by using a single instruction. This feature allows for the power management as well as the emulation mode to be defined simultaneously. There is neither evidence nor motivation suggesting that the behavior of a power management controller as well as the mode of emulation of the controller should be affected in this fashion, especially when it reduces the number of instructions available for other processor-critical functions. Accordingly, it would not have been obvious to a person of ordinary skill in the art to modify Yoshida in view of Gaglani to arrive at the invention as claimed.

Concerning Claim 14, Yoshida discloses:

A method of operating a data processing apparatus (Column 4, Lines 62-63) to test power management instructions, comprising the steps of:

(a) executing on a processor a command power management instruction to generate command data (Table 11, Columns 24, Lines 52-53);

(b) issuing said command data to a power management controller (Figure 1, Item PR; Column 4, Lines 62-65);

(c) controlling, via the power management controller, power management logic to perform an associated set of power management functions dependent on said command data (Column 5, Lines 8-11), the data processing apparatus having first power management logic controllable by the power management controller (Column 5, Lines 32-36), and the power

management controller having an interface to enable communication with additional power management logic (Figure Column 5, Lines 32-36);

Yoshida does not disclose an emulation mode for the power management controller. As a result, he does not disclose the processor being able to affect both the power management functions and the emulation mode of the power management controller according to a power management instruction. Nor does Yoshida disclose the power management functions executed being dependent upon the emulation mode of the power management controller.

Gaglani teaches:

at said step (c), said power management controller (Columns 2 and 5-6, Lines 27-30 and 65-67 to 1, respectively; although Gaglani does not specifically teach of a power management controller, he extends his teachings to other circuits, of which a power management controller may be included without changing the principles behind his teachings) being arranged when said emulation mode is not set to initiate said associated set of power management functions dependent on said command data (Figure 3A; Column 5, Lines 12-29), and being arranged when said emulation mode is set to only initiate a subset of said associated set of power management functions not requiring communication over said interface (Column 6, Lines 10-15).

Gaglani provides as partial motivation that "one objective of testing is providing individual access to the carious functionalities and hardware elements of the device, so that the performance characteristics thereof can be evaluated" (Column 1, Lines 35-38). Although Gaglani does not cite a power management controller, it is clear that the principles he expresses in his motivate that his teachings may be applied to a power management controller in a data processing apparatus. Therefore, it would have been obvious to a person of ordinary skill in the

art to combine the teachings of Gaglani with the device disclosed by Yoshida for the purposes of providing a simple way for testing the correctness of the power management controller.

Gaglani, however, does not teach of affecting both the operation of the circuit as well as the emulation mode of the circuit by using a single instruction. This feature allows for the power management as well as the emulation mode to be defined simultaneously. There is neither evidence nor motivation suggesting that the behavior of a power management controller as well as the mode of emulation of the controller should be affected in this fashion, especially when it reduces the number of instructions available for other processor-critical functions. Accordingly, it would not have been obvious to a person of ordinary skill in the art to modify Yoshida in view of Gaglani to arrive at the invention as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ramirez provides a test method for a circuit similar to Gaglani that allows an emulation mode to be set and behavior of the system changed according to the mode so that individual components of a device may be tested separately.

Ito teaches of a circuit that may be put into a test mode and, according to the mode, at least a portion of the circuit may be inactivated.

Shah teaches of a debugging component to power management functions but does not provide an instruction that commands both elements of the system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Henry whose telephone number is (571) 272-3845. The examiner can normally be reached on Monday - Friday (8:00 am -5:00 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MAH

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